CMI-8738/PCI C3D*X*
PCI-Based HRTF 3D Extension Positional Audio Chip

Features

- **HRTF-based 3D positional audio, supporting DirectSound™ 3D and A3D™ interface**
- **Supports rear side speakers, C3D*X* positional audio in 4 CH speaker mode**
- **Legacy audio SB16™ compatible**
- **DLS-based wavetable music synthesizer, supports DirectMusic™**
- **Professional digital audio interface supporting 24-bit SPDIF IN and OUT (44.1K and 48K format)**
- **Built-in 32ohm Earphone buffer**
- **Built-in PCtel® HSP56 Modem™ interface**
- **Drivers support AC3® 5.1CH interface.**
- **MPU-401 port**
- **Dual game port**
- **16-bit full duplex CODEC**
- **4 CH 16-bit DAC**
- **32-bit PCI bus master**
- **External E²PROM interface**
- **Single chip design, +5V, 128 pins QFP**

With high speed PCI V2.1 bus controller and legacy audio SB16® DSPemulator,CMI8738 is designed for PC add-in cards and all-in-one motherboards. No external CODEC is needed in CMI8738: CMI-8738 supports the legacy audio – SB16™, FM emulator/DLS wavetable music synthesis, and HRTF 3D positional audio functions. Above all CMI8738 supports PCtel® HSP56 (1789) interface.

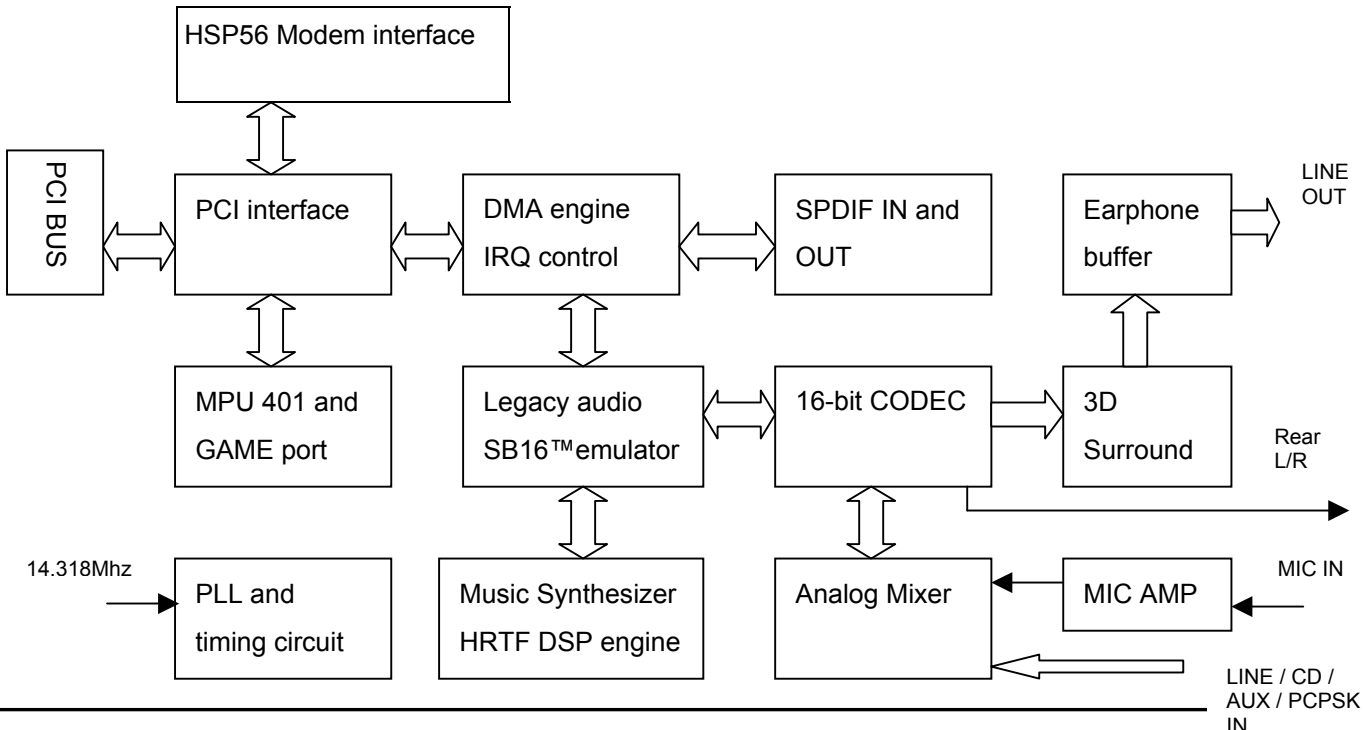
Being compatible with A3D™ and DirectSound™ 3D, CMI8738 meets PC98® requirements, and supports professional digital audio interface such as 24-bit SPDIF IN (0.5V ~ 5V)and OUT(44.1K and 48K format).

CMI8738 uses HRTF 3D extension technology to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four- speaker one(it supports additional 2CH 16-bit DAC to provide rear side audio). It greatly improves HRTF 3D positional audio quality and successfully removes the sweet spot limitations: users can enjoy genuine 3D audio gaming effects, and don't have to worry about the environmental confinement any more.

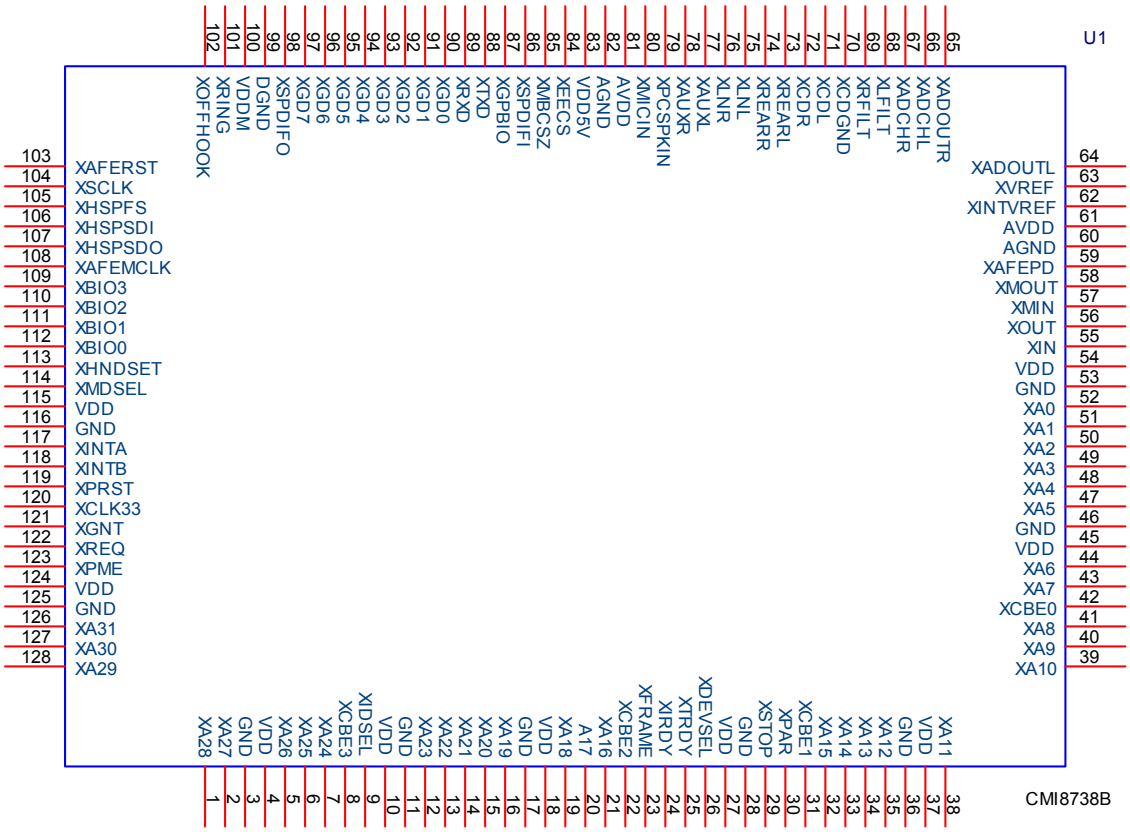
Being outstanding for its full audio functions, competitive price, and power management, CMI-8738 is the best choice for people seeking for optimum use of the PC applications.

C-Media licensed HRTF 3D library from Central Research Lab (CRL®), U.K, who provides one of the world's best HRTF libraries (CRL® also licensed its audio technology to YAMAHA®, ESS®, and other well-known sound chip makers).

CMI-8738/PCI Block Diagram



PINOUT



CMI8738/PCI C3DX AUDIO CHIP
QFP 128 PINS

DIGITAL PIN DESCRIPTION

Name	Number	PIN Type	Definition
XA31-XA0	126-128,1-2,5-7,12-16,19-21,32-35,38-41,43-44,47-52	I/O	PCI bus address and data lines
XINTA	117	O	Interrupt request , active-low.
XINTB	118	O	Modem Interrupt request,active-low
XPRST	119	I	Reset
XCLK33	120	I	PCI bus clock.
XGNT	121	I	Bus master grant, active-low.
XREQ	122	O	Bus master request, tri-state output, active-low.
XIDSEL	9	I	ID select, active-high.
XFRAME	23	I/O	Cycle frame, active-low.
XIRDY	24	I/O	Initiator ready, active-low. The bus master device is ready to transmit or receive data
XTRDY	25	I/O	Target ready, active-low. The target device is ready to transmit or receive data
XDEVSEL	26	I/O	Device select, active-low. The target device has decoded the address of the current transaction as its own chip select range.
XSTOP	29	I/O	Stop transaction, active-low. The target device request to the master to stop the current transaction.
XPAR	30	I/O	Parity. The pin indicates even parity across XA31-XA9 and XCBE3-0 for both address and data phases.
XCBE3,2,1,0	8,22,31,42	I/O	Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction.
VDD	4,10,18,27,37,45,54,115,124	+5V	Digital and PCI I/O power pin
GND	3,11,17,28,36,46,53,116,125	GND	Digital and PCI I/O ground
XIN	55	I	14.318Mhz crystal, or external clock input
XOUT	56	O	14.318Mhz crystal
XGD7-XGD4	97-94	I	Game port switch input pin. Switch D to switch A
XGD3-XGD0	93-90	I/O	Game port resistor input pin. RC3 to RC0
XTXD	88	O	MIDI transmit data
XRXD	89	I	MIDI receive data
XSPDIFO	98	O	44.1kHZ SPDIF output
XSPDIFI	86	I*	44.1kHZ SPDIF input
XSCLK	104	O	MODEM DAA serial clock
XBIO3-XBIO0	109-112	I/O	General purpose I/O
VDD5V	83	+5V	Digital and PCI I/O power pin
VDDM	100	+5V	Digital and PCI I/O power pin
DGND	99	GND	Digital and PCI I/O ground
XEECS	84	O	EEPROM chip select

ANALOG PIN DESCRIPTION

AVDD	**61,81**	**+5V**	**Analog power**
AGND	**60,82**	**GND**	**Analog ground**
XADOUTL-R	**64,65**	**AO1**	**Line out**
XADCHL-R	**66,67**	**AI/O**	**ADC filter**
XLFILT	**68**	**AI/O**	**Left channel DAC filter**
XRFILT	**69**	**AI/O**	**Right channel DAC filter**
XINTVREF	**62**	**AI**	**Reference Voltage**
XVREF	**63**	**AI**	**Reference Voltage (no use, left it floating)**
XCDL-R XCDGND	**71,72,70**	**AI**	**CD audio differential input**
XLNL-R	**75,76**	**AI**	**Line in or Rear speaker out**
XAUXL-R	**77,78**	**AI**	**Aux. Line in**
XPCSPKIN	**79**	**AI**	**PC beep signal**
XMICIN	**80**	**AI**	**Microphone in**
XREARL-R	**73,74**	**AI/O**	**Rear speaker out**
XMDSEL	**114**	**I**	**Modes chip select (high:enable)**
XGPBIO	**87**	**O**	**General purpose I/O pin (0=disabled, 1=enabled)**
XRING	**101**	**I**	**Ring detection input**
XOFFHOOK	**102**	**O**	**Off-hook control output**
XAFERST	**103**	**O**	**Reset signal for MODEM DAA**
XHSPFS	**105**	**O**	**MODEM DAA frame SYNC**
XHSPSDI	**106**	**I**	**MODEM DAA data input**
XHSPSDO	**107**	**O**	**MODEM DAA data output**
XAFEMCLK	**108**	**O**	**MODEM DAA master clock**
XHNDSET	**113**	**O**	**Reserved**
XAFEPD	**59**	**O**	**Reserved**
XMOUT	**58**	**O**	**MODEM crystal output (18.432MHz)**
XMIN	**57**	**I**	**MODEM crystal input**
XMBCSZ	**85**	**I**	**Audio chip select (low:enable)**

POWER ON CONFIGURATION PIN

Name	Number	Definition
XTXD	88	When pull-down select add-on mode, default pull-high motherboard.
XAFEPD	59	When pull-down enable #INTB share with #INTA, default high disabled.
XHNDSET	113	When pull-down enable external 18.432Mhz x'tal to HSP module, default pull-high enable internal 24.576Mhz to HSP module.
XBIO0	112	When pull-down select CLKGEN ref. clock to external 24.576Mhz x'tal. default pull-high select 14.318Mhz

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Digital power voltage	VDD	VDD±5%	V
Analog power voltage	AVDD	AVDD±5%	V
Operating temperature range	TO	0 to 70	°C
Storage temperature range	TST	-40 to 125	°C
Maximum power dissipation	PDMAX	300	MW

Digital Characteristics

PARAMETER	Symbol	Min	Typ	Max	Unit
Input high voltage(PCI I/O)	VIH	2.		VDD+0.5	V
Input low voltage (PCI I/O)	VIL	-0.5		0.8	V
Output high voltage	VOH	2.4		VDD	V
Output low voltage	VOL	0.0	0.2	0.4	V
SPDIF IN input high voltage	VIH1		2.6		V
SPDIF IN input low voltage	VIL1		2.4		V
SPDIF output high voltage	VOH1		VDD		V
SPDIF output low voltage	VOL1		VSS		V
Output buffer current			5		mA

Audio Characteristics

PARAMETER	Symbol	Min	Typ	Max	Unit
Analog input voltage	Avin		1.1		VRms
Analog output voltage	Avout		1.1		VRms
A-A S/N ratio			85		db
A-A THD			0.09		
ADC S/N ratio			80		db
ADC THD			0.1	0.2	%
DAC S/N ratio			80		db
DAC THD			0.1	0.2	%
SPDIF IN/OUT S/N ratio			120		db
SPDIF IN/OUT THD			0		%
Microphone input level		20		200	mv
Microphone booster				20	db

CMI8738 PCI Configuration Spaces(Audio)

00h 13F6 : (**Vender ID**) read only

02h 0111 : (Device ID) read only

04h 0006 : Command (State after #RST all is "**0**")

0 (bit 9) Fast back-to-back enable

0 (bit 8) #SERR enable (R/W)

0 (bit 7) Wait cycle control

0 (bit 6) Parity error response

0 (bit 5) VGA palette snoop

0 (bit 4) Memory write and invalidate enable

0 (bit 3) Special cycles

1 (bit 2) Bus master **(R/W)**

0 (bit 1) **Memory space**

1 (bit 0) I/O space **(R/W)**

06h 0280 : Status

0 (bit 15) Detected Parity Error

0 (bit 14) Signaled System Error

0 (bit 13) Received Master Abort

0 (bit 12) Received Target Abort

0 (bit 11) Signaled Target Abort

01 (bits 10-9) **DEVSEL timing** 00-fast, 01-medium, 10-slow

0 (bit 8) Data Parity Error Detected

1 (bit 7) **Fast Back-to-Back Capable**

0 (bit 6) UDF Supported

0 (bit 5) 0-33MHz ,1-66MHZ Capable

00000 (bits 4-0) Reserved

08h 10 : Revision ID

09h 040100 : Audio device

0Ch 00 : Cache Line Size

0Dh 20 : **Latency Timer**

0Eh 80 : Header Type

0Fh 00 : BIST

10h 0000d401 : I/O of length : -65280(ffff0100h) : First Base Address register
14h 00000000 : Uninitialized : Second Base Address register
18h 00000000 : Uninitialized : Third Base Address register
1Ch 00000000 : Uninitialized : Fourth Base Address register
20h 00000000 : Uninitialized : Fifth Base Address register
24h 00000000 : Uninitialized : Sixth Base Address register
28h 00000000 : Cardbus CIS Pointer
2Ch 13f6 : (**SubSystem Vender ID**) (R/W)
2Eh ffff : **SubSystem ID** (R/W)
30h 00000000 : Expansion ROM Base Address
34h 00000000 : Reserved
38h 00000000 : Reserved
3Ch 05 : **Interrupt Line**
3Dh 01 : **Interrupt Pin**
3Eh 02 : **Min Grant**
3Fh 18 : **Max Latency**

CMI8738 Configuration Spaces(Modem)

00h 13F6: (Vender ID) read only
02h 0211: (Device ID) read only
04h Command (State after #RST all is "0")
- 0 (bit 9) Fast back-to-back enable (read only)
- 0 (bit 8) #SERR enable (Read only)
- 0 (bit 7) Wait cycle control (read only)
- 0 (bit 6) Parity error response (read only)
- 0 (bit 5) VGA palette snoop (read only)
- 0 (bit 4) Memory write and invalidate enable (read only)
- 0 (bit 3) Special cycles (read only)
- 0 (bit 2) Bus master (read only)
- 1 (bit 1) Memory space (R/W)
- 0 (bit 0) I/O space (read only)

06h Status
- B0 (bit 15) Detected Parity Error
- B0 (bit 14) Signaled System Error

B0 (bit 13) Received Master Abort
B0 (bit 12) Received Target Abort
B0 (bit 11) Signaled Target Abort
B01 (bits 10-9) DEVSEL timing 00-fast, 01-medium, 10-slow
B0 (bit 8) Data parity Error Detected
B0 (bit 7) Fast Back-to-Back Capable
B0 (bit 6) UDF Supported
B0 (bit 5) 0-33MHz, 1-66MHz Capable
B00000 (bits 4-0) Reserved

08h X10: Revision ID
09h X078000: Communication device (Modem)
0Ch X00: Cache Line Size
0Dh X00: latency Timer
oEh X80: Header Type (Multifunction device)
oFh X00: BIST
10h Xbbbbb000: Allocate 4K memory space.
14h X00000000: not used - Second Base Address register
18h X00000000: not used - Third Base Address register
1Ch X00000000: not used- Four Base Address register
20h X00000000: not used- Fifth Base Address register
24h X00000000: not used- Sixth Base Address register
28h X00000000: Card bus CIS Pointer
2Ch X13f6: Sub-System Vender ID (Value can be replaced after reset.) (R/W)
2Eh X0211: Sub-System ID (Value can be replaced after reset) (R/W)
*Refer to the Audio PCI registers bit-13 of address (18-1B) for how to replace.
30h X00000000: Expansion ROM Base Address
34h X00000040: pointer to the power-saving registers. (Read only)
38h X00000000: Reserved
3Ch X00: Interrupt Line (R/W)
3Dh Interrupt Pin(X01 share interrupt/X02 not share interrupt with Audio)
*Select from the power on pin configuration
3Eh X00: Min Grant(not used)
3Fh X00: max Latency(not used)
40h XEC4A0001(read only)

44h-47h

B0-B1: PMST (R/W) (11)

B7-B2: all 0 (read only)

B8: PMEEN (R/W) (Sticky bit)

B12-B9: DSEL (R/W) 0000

B14-B13: all 0 (read only)

B15: PMESTS (Sticky bit)

Internal Register Mapping

Function Control Register 0

Address **00**H

Bit(s)	R/W	Name	Description
31-20		Reserved.	
19		RST_CH1	Channel1, 1->Reset (Default 0)
18		RST_CH0	Channel0, 1->Reset (Default 0)
17		CHEN1	Channel1, 1->Enabled, 0->Disabled.
16		CHEN0	Channel0, 1->Enabled, 0->Disabled.
15-4		Reserved	
3		PAUSE1	Channel1, 1->Pause if channel1 is enabled.
2		PAUSE0	Channel0, 1->Pause if channel0 is enabled.
1		CHADC1	Channel 1 , 1->Recording, 0->Playback
0		CHADC0	Channel 0, 1->Recording, 0->Playback

Function Control Register 1

Address **04**H

Bit(s)	R/W	Name	Description
31-16		Reserved	
15-13		DSFC[2:0]	**DAC** Sampling Frequency Select,
		0 0 0	5.512 K
		0 0 1	11.025 K
		0 1 0	22.05 K
		0 1 1	44.1 K
		1 0 0	8 K
		1 0 1	16 K
		1 1 0	32 K
		1 1 1	48 K
12-10		ASFC[2:0]	**ADC** Sampling Frequency Select,
		0 0 0	5.512 K
		0 0 1	11.025 K
		0 1 0	22.05 K
		0 1 1	44.1 K
		1 0 0	8 K

	1	0	1	16 K
	1	1	0	32 K
	1	1	1	48 K

9 SPDF_1 SPDIF IN/OUT at Channel B at 44.1K double-words/sec.

8 SPDF_0 SPDIF OUT only at Channel A at 44.1K double-words/sec.

7 SPDFLOOP external SPDIF/IN loopback to external SPDIF/OUT .

6 SPDO2DAC SPDIF/OUT can be heard from internal DAC.

5 INTRM Interrupt Mask bit for MCB (Master control block) module interrupt.

0 MCB interrupt disabled.

1 MCB interrupt enabled.

4 BREQ If this bit is set low it will prevent the MCB and DAC/ADC block from accessing the memory.

0 Bus Master request disabled(power on state)

1 Bus Master request enabled.

3 VOICE_EN This bit enables Legacy Voice device(SB16,FM).

0 Legacy Voice disabled on channel 0.

1 Legacy Voice enabled on channel 0.

2 UART_EN This bit enables Legacy UART device.

0 UART disabled

1 UART enabled

1 JYSTK_EN This bit enables Legacy Joystick device.

0 Joystick disabled

1 Joystick enabled

0 Reserved

Channel Format Register

Address **08**H

Bit(s)	R/W	Name	Description
31-24		VER[7:0]	PCI Audio subversion for internal indentification. “01”
23-22		SWTCLK[1:0]	In real mode, switch CLOCK Generator output to XSPDIF/out.
			0X maintain original spdif/out bit stream to XSPDIF/out.
			10 16.9344MHZ to I/O XSPDIFO
			11 24.576MHZ to I/O XSPDIFO
21		Reserved	
20		AC3EN	When set 1,it will generate AC3 enable bit on spdif/out FRAMA #1 bit 30 (channel status bit)

19	SELSPDIFI2	When set 1,internal spdif/in will switch to secondary SPDIF/IN I/O(XHNDSET)
18	FMOFFSET2	When set 1 and Reg. 24H bit7 'FMmute=1',FM PCM will be forced to DC value 0002H.
17	SPD24SEL	When set 1 and SPD32SEL=1,SPDIF/out transmit 24bit PCM data,PCM data in system format only valid in 24 least significant Bits D[23:0] ,bits D[31:24] don't care.
16	INVSPDIFI	Inverse spdif/in data,function for compatible to different CD-ROM .
15-14	AdcBitLen[1:0]	Sample resolution
	00	16 Bits per sample . (Default)
	01	15 Bits per sample.
	10	14 Bits per sample.
	11	13 Bits per sample.
13-12	AdcDacLen[1:0]	Sample resolution
	00	600nSec per bit in a sample.
	01	660nSec per bit in a sample.
	10	1.3uSec per bit in a sample. (Default)
	11	2.8uSec per bit in a sample.
11	CH1 Ssmple Rate 176K	
10	CH1 Sample Rate 88K	
9	CH0 Sample Rate 176K	
8	CH0 Sample Rate 88K	
7-4	reserved	
3-2	CH1FMT[1:0]	Data format of channel 1
	00	8 bit Mono mode
	01	8 bit Stereo mode
	10	16 bit Mono mode
	11	16 bit Stereo mode
1-0	CH0FMT[1:0]	Data format of channel0
	00	8 bit Mono mode
	01	8 bit Stereo mode
	10	16bit Mono mode
	11	16 bit Stereo mode

Interrupt Hold/Clear Register

Address **0C**H

Bit(s)	R/W	Name	Description

31-19	Reserved	
18	TDMA_INT_EN	Interrupt hold/clear bits for updating TDMA position
	0	Interruupt Clear
	1	Interrupt Hold if exist.
17	CH1_INT_EN	Interrupt hold/clear bits for the Channel 1.
	0	Interrupt Clear
	1	Interrupt Hold if exist.
16	CH0_INT_EN	Interrupt hold/clear bits for the Channel 0.
	0	Interrupt Clear
	1	Interrupt Hold if exist.
15-0	Reserved	

Interrupt Register

Address **10**H

Bit(s)	R/W	Name	Description
31	R	INTR	Interrupt reflected from any sources.
			0 No interrupt
			1 Interrupt pending
30-28		Reserved	
27	R	VCO	
26	R	MCBint	Abort conditions occur during PCI Bus Target/Master Access.
			0 No interrupt
			0 Interrupt pending
25-17		Reserved	
16	R	UARTint	This bit is the UART interrupt bit.
			0 No UART interrupt
			1 UART interrupt pending
15	R	LTDMAINT	Interrupt for updating Low Channel TDMA position.
			0 No interrupt
			1 Interrupt pending
14	R	HTDMAINT	Interrupt for updation High Channel TDMA position.
			0 No interrupt.
			1 Interrupt pending.
13-8		Reserved	
7	R	XDO46	Direct programming EEPROM interface , read data register
6	R	LHBTOG	High/Low status from DMA CTRL register.
5	R	LegHDMA	Legacy is in High DMA channel.

4	R	LegStereo	Legacy is in Stereo mode.
3	R	Ch1Busy	Channel B Busy.
2	R	Ch0Busy	Channel A Busy.
1	R	Chint1	Channel B Interrupt.
			0 No interrupt
			1 Interrupt pending
0	R	Chint0	Channel A Interrupt.
			0 No interrupt
			1 Interrupt pending

Legacy Control/Status Register

Address **14**H

Bit(s)	R/W	Name	Description
31		Reserved	
30-29		VMPU [1:0]	Base address for MPU401 access
			00 Base address : 330h
			01 Base address : 320h
			10 Base address : 310h
			11 Base address : 300h
28		Reserved	
27-26		VSBSEL[1:0]	The Base Address Select for SB16 access.
			00 Base address: 220h
			01 Base address: 240h
			10 Base address: 260h
			11 Base address: 280h
25-24		FMSEL[1:0]	The Base Address Select for FM access.
			00 Base address : 388h
			01 Base address : 3C8h
			10 Base address : 3E0h
			11 Base address : 3E8h
23		ENSPDOUT	enable XSPDIF/OUT to I/O Interface
22		SPDCOPYRHT	SPDIF IN/OUT CopyRight status bit
21		DAC2SPDO	enable Wave+FM+MIDI to SPDIF/OUT interface
20		SetRetry	Mode of wait state . 0:legacy I/O wait (default) 1:legacy I/O BUS retry
19		C_EEACCESS	Direct programming EEPROM interface Registers.
18		C_EECS	
17		C_EEDI46	

16	C_EECK46
15-0	Reserved

Micellaneous Control Register

Address 18H

Bit(s)	R/W	Name	Description
31		PWD	Power Down Mode enabled..
30		RESET	Reset Bus Master/DSP Engine.
29-28		SFIL[1:0]	Four level of filter control at the front end DAC..
27		TX/VX	Which motherboard to work with 0 VX chip sets. 1 TX chip sets.
26		N4SPK3D	Hardware copy front channel to rear channel
25		SPDO5V	SPDIF-out level setting
24		W / SPDIF48K ; R / SPATUS48K ;	
23		ENDBDAC	Default low, High will enable Double DAC structure.
22		XCHGDAC	Default low, 0 CH0 > Front SPKR, CH1 > Back SPKR. 1 CH0 > Back SPKR, CH1 > Front SPKR.
21		SPD32SEL	when high, support 32bits SPDIF format ,low 16bits
20		SPDFLOOPI	internal SPDIF/OUT loopback to internal SPDIF/IN, for loopback testing
19		FM_EN	Legacy FM enabled.
18		Reserved	
17		Reserved	
16		VIDWPDSB	Sub ID write protect disabled. (default 0)
15		SPDF_AC97	0: SPDIF/OUT 44.1K 1:SPDIF/OUT 48K(share with AC97 transfer)
14		MASK_EN	Activate channel mask on Legacy DMA. 0 Disabled 1 Enabled
13		VIDWPDSB	Write Protect of HSP Configuration Sub ID. 0 Protect. 1 No protect.
12		SFILENB	Let software contrl filter stepping at the front end DAC.
11-9		Mmode[2:0]	Modem DAA interface mode selection,default 000 000 Modem in Local DAA interface mode 001 Modem in AC97_LINK mode

			010 Modem in parallel CM_LINK mode (external modem bridge supported) 1XX Modem in serial CM_LINK mode (external modem bridge supported)
8		Reserved	
7		FLINKON	force Link detection on when in CM_LINK mode,default 0
6		FLINKOFF	force Link detection off when in CM_LINK mode,default 0
5		Reserved	
4		MIDSMP	Enable 1/2 interpolation at the Front end DAC..
3-2		UPDDMA[1:0]	For every the number of samples to notify updating TDMA position.
			00 Every 2048 samples
			01 Every 1024 samples
			10 Every 512 samples.
			11 Every 256 samples.
1-0		TWAIT[1:0]	For controling the length of legacy BUS cycle.
			00 3 PCICLK.
			01 18 PCICLK.
			10 24 PCICLK
			11 32 PCICLK
* Notice	REQ_SQ[2:0]		States of BusRequest Engine.
	MM_DATA		Bus Master is using Bus.
	MIDLE		Bus Master is not using Bus.
	REQA/REQB		Channel 0/1 BusMaster Request.
	GNTA/GNTB		Channel 0/1 BusMaster Grant.
	ADRQ/BDRQ		Channel 0/1 DMA Request.
	ADACK/BDACK		Channel 0/1 DMA Acknoledge.
	AIRQ/BIRQ		Channel 0/1 Interrupt.
	CX/BX		Channel 0/1 Busy.

T - DMA Position

Address **1CH**

Bit(s)	R/W	Name	Description
31-16	R	TDMACN T	Current Byte/Word Count of DMA channel.
15-0	R	TDMAADR	Current Address of DMA channel.

Mixer Control / Device Configure Register (can be accessed only by **BYTE**

instruction)

Address **20**H

Bit(s)	R/W	Name	Description
7-0	W	SBVR[7:0]	Programmable SB16 version No.
	R	DEV[7:0]	Hardwire device version No.

Address **21**H

Bit(s)	R/W	Name	Description
7-3		Reserved	
2		X_ADPCM	SB16 ADPCM enable,default disabled.
1		PROINV	SBPro Left/Right channel switching.
0		X_SB16	Indicate device active as SB16 compatible, default SB16

Address **22**H

Bit(s)	R/W	Name	Description
7-0		IDXdata	Mapping SB compatible mixer INDEX register data port(A2x5h)

Address **23**H

Bit(s)	R/W	Name	Description
7-0		IDXaddr	Mapping SB compatible mixer INDEX register address port(A2x4h)

Address **24**H

Bit(s)	R/W	Name	Description
7		Fmmute	Mute FM
6		Wsmute	Mute Wave stream
5		SPK4	select four speaker mode(emulate Line in to Line out)
4		Rear2front	exchange rear and front channels's speaker out
3		Waveinl	Digital Wave recording Left channel
2		Waveinr	Digital Wave recording Right channel
1		X3DEN	3D surround enable.
0		Cdplay	SPDIF/IN PCM to DAC enable

Address **25**H

Bit(s)	R/W	Name	Description
7		RAUXREN	Recording source select R-Aux
6		RAUXLEN	Recording source select L_Aux

5		VAUXRM	R-AUX mute control
4		VAUXLM	L-AUX mute control
3-1		VADMIC[2:0]	Recording MIC volume control
0		MICGAINZ	MIC gain control,default high disable

Address **26**H

Bit(s)	R/W	Name	Description
7-4		VAUXL[3:0]	L-AUX volume control
3-0		VAUXR[3:0]	R-AUX volume control

Address **27**H

Bit(s)	R/W	Name	Description
0		DMAUTO	SB16 Low/High DMA Auto detect enabled ,When high.
1		SPDVALID	SPDIF/IN valid bit detect enabled, When high.
2		XGPBIO	general purpose bi-direction pin, when high output tri-state (default LOW)
3		Reserved	
4		Reserved	
5		XGPO1	general purpose output pin 1,this pin shared with XSPDIFO pin, and enabled when index reg. F0_bit 0 programmed high.
6-7		Reserved	

Mup401 PCI Port

Index address

40-4FH

FM PCI Port

Index address

50-5FH

Extension Index Register (access from SB compatible mixer port)

Index address **F0**H

Bit(s)	R/W	Name	Description
7-5		VPHONE[2:0]	Phone volume control
4		VPHOM	Phone mute control
3		VSPKM	PC-Speaker mute control,default high unmute
2		RLOOPREN	Recording R-channel enable
1		RLOOPLEN	Recording L-channel enable
0		VADMIC3	Micphone record boost, default low disable, high enable.

Index address **F8-FF**H

These 8 registers is used to programming M/N conunter by clock generator

Channel 0 Frame Register 1

Address **80**H

Bit(s)	R/W	Name	Description
31-0	W	BASADDR0	Base address of channel 0.
	R	CURADDR0	Current address of channel 0.

Channel 0 Frame Register 2

Address **84**H

Bit(s)	R/W	Name	Description
31-16	W	BASCNT0	Base count of samples at Codec.
15-0	W	BASCNT0	Base count of samples at Bus Master.
31-16	R	CURCNT0	Current count of samples at Codec.
15-0	R	CURCNT0	Current count of samples at Bus Master.

Channel 1 Frame Register 1

Address **88**H

Bit(s)	R/W	Name	Description
31-0	W	BASADDR1	Base address of channel 0.
	R	CURADDR1	Current address of channel 0.

Channel 1 Frame Register 2

Address **8C**H

Bit(s)	R/W	Name	Description
31-16	W	BASCNT1	Base count of samples at Codec.
15-0	W	BASCNT1	Base count of samples at Bus Master.
31-16	R	CURCNT1	Current count of samples at Codec.
15-0	R	CURCNT1	Current count of samples at Bus Master.

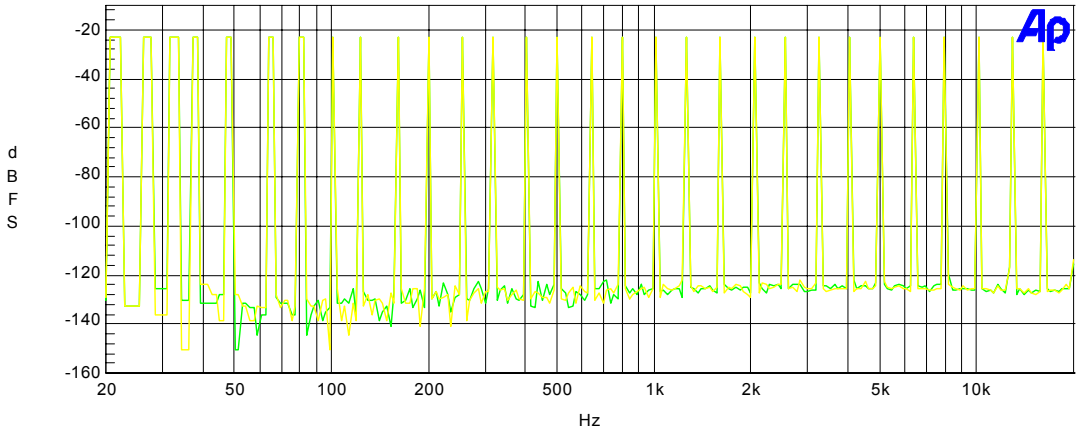
Legacy SB compatible mixer

Index	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved							
0x04	Wave volume left channel				Wave volume right channel			
0x0A						Mic volume		
0x22	Master volume left channel				Master volume right channel			
0x26	FM volume left channel				FM volume right channel			
0x28	Analog-CD volume left channel				Analog-CD volume right channel			
0x2E	Line-in volume left channel				Line-in volume right channel			
0x30	Reserved							
0x31	Reserved							
0x32	Reserved							
0x33	Reserved							
0x34	Reserved							
0x35	Reserved							
0x36	Reserved							
0x37	Reserved							
0x38	Reserved							
0x39	Reserved							
0x3A	Reserved							
0x3B	PC spk volume							
0x3C				Output muting controls				
				Line L	Line R	CD L	CD R	Mic
0x3D		Recording left channel controls						
		FM L	FM R	Line L	Line R	CD L	CD R	Mic
0x3E		Recording right channel controls						
		FM L	FM R	Line L	Line R	CD L	CD R	Mic
0x3F	Reserved							
0x40	Reserved							
0x41	Reserved							
0x42	Reserved							
0x43	Reserved							
0x44	Reserved							
0x45	Reserved							
0x46	Reserved							
0x47	Reserved							
0x80					IRQ channel (read only)			
					IRQ10	IRQ7	IRQ5	IRQ2(9)
0x81	16 bit DMA channel (read only)				8 bit DMA channel (read only)			
	DMA 7		DMA 5		DMA 3		DMA 1	DMA 0
0x82						Interrupt status (read only)		
						MPU-401	16bit DMA	8bit DMA

- Please do not write any values into reserved registers

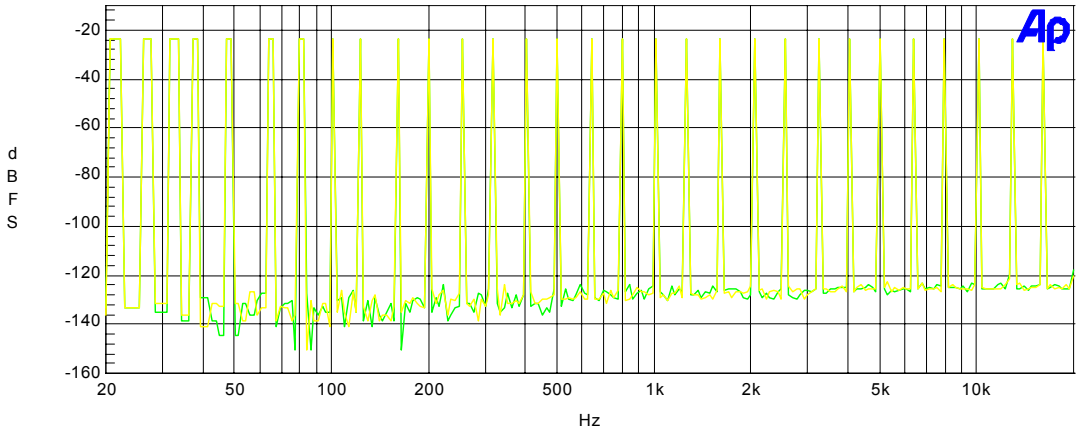
CMI8738 SPDIF IN/OUT Test Report

CMI8738 SPDIF-out Frequency, Distortion Noise Response 03/04/99 12:19:31



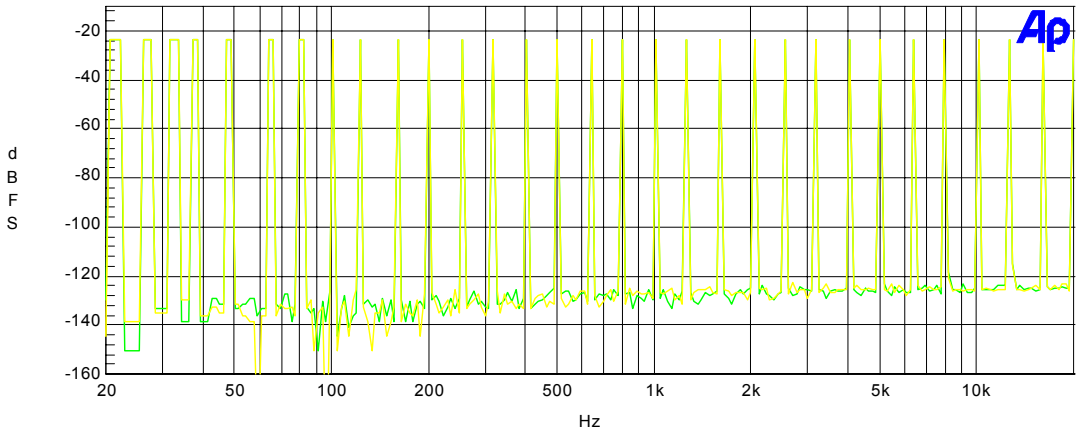
Color	Line Style	Thick	Data	Axis
Green	Solid	1	Fasttest.Ch.1 Ampl	Left
Yellow	Solid	1	Fasttest.Ch.2 Ampl	Left

CMI8738 SPDIF-in Frequency, Distortion Noise Response 03/04/99 14:11:15



Color	Line Style	Thick	Data	Axis
Green	Solid	1	Fasttest.Ch.1 Ampl	Left
Yellow	Solid	1	Fasttest.Ch.2 Ampl	Left

CMI8738 SPDIF-through Frequency, Distortion Noise Response 03/04/99 12:36:04



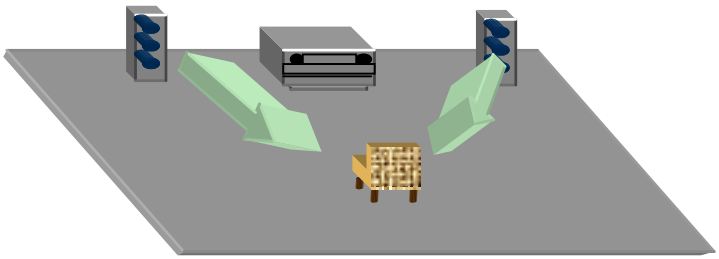
Color	Line Style	Thick	Data	Axis
Green	Solid	1	Fasttest.Ch.1 Ampl	Left
Yellow	Solid	1	Fasttest.Ch.2 Ampl	Left

1. **SPDIF OUT (playback) > 120db**
2. **SPDIF IN (recording) > 120db**
3. **SPDIF through mode (bypass) > 120db**

* This report is generated by Audio Precision® System II using multi-tone mode.

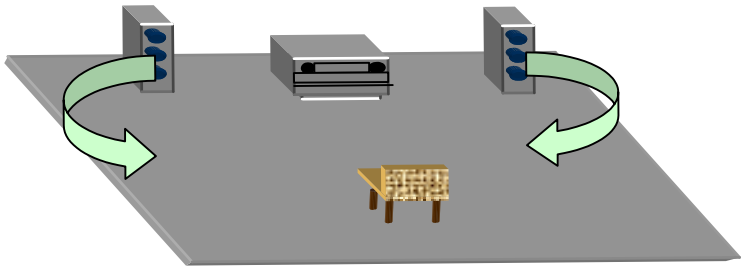
1. Stereo

It is only one-dimensional, as sounds come from (left /right) the physical location of speakers.



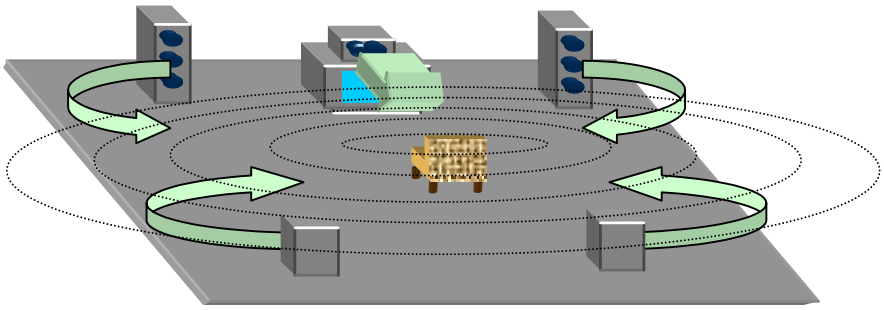
2. Surround (Stereo Expander)

It filters the existing stereo signal to make the sounds fill in the area around the speakers, and in front of the listener. Sound sources appear to come from outside the physical locations of the speakers.



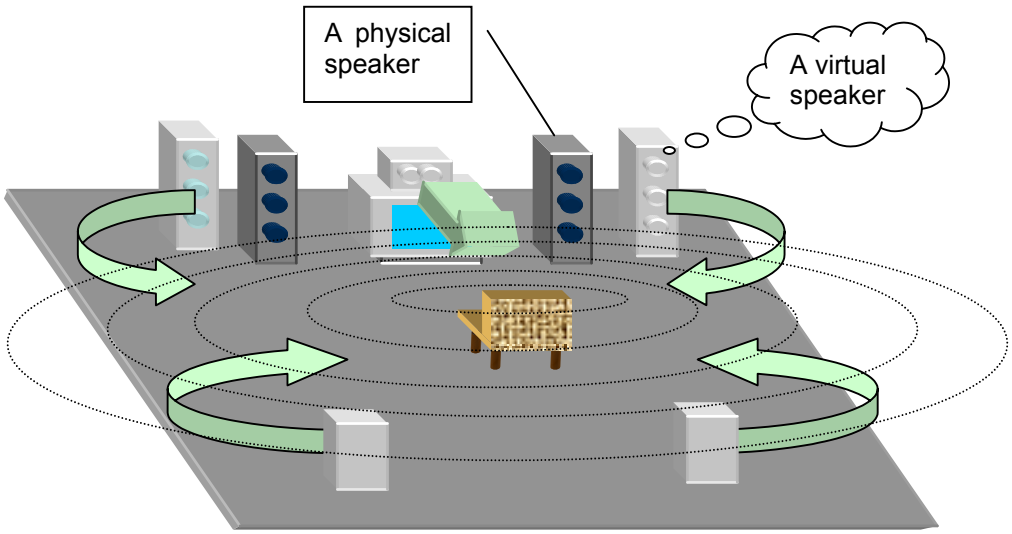
3. Multi-Speaker Surround (Dolby Pro Logic or Digital AC-3)

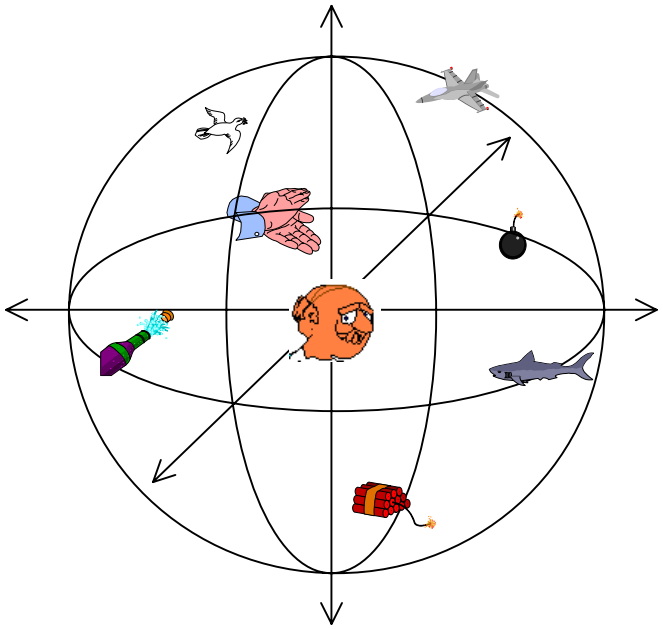
It uses five speakers instead of two to surround the listener; hence, sound sources come from five directions and create engaging audio experience. This surround sound effect, however, has to be pre-recorded, and it dose not support interactive environment.



4. HRTF 3D Positional 3D (C-Media 3D)

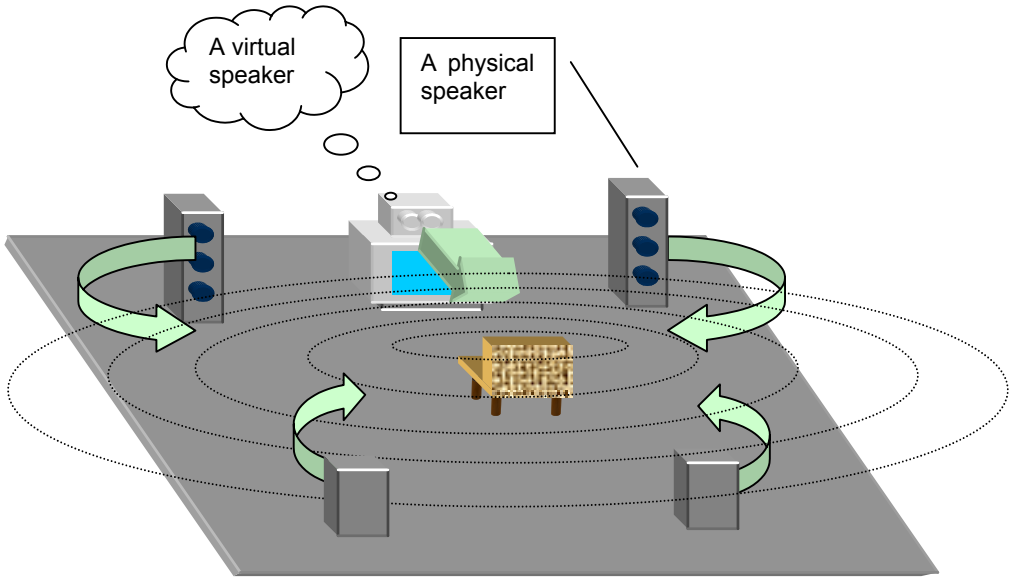
Only this sound processing technology can be called real 3D manifestation, as 3D usually refers to the three dimensions of X, Y and Z. This technology allows people to pin-point the location of sound in the real world (up/down, left/right, front/back)using only two speakers or a pair of headphones. This technology also supports interactive 3D applications to get a real-time placement of sounds via API (application programming interface) such as Microsoft DirectSound3D™. We can also use this technology to simulate Multi-speaker Surround with two physical speakers to deliver five “virtual" speakers in the air, surrounding the listener and creating home theater sound environment. This is the most economical and the easiest solution to people who would like to get high performance surround sound but don’t want to spend money in adding extra speakers.





5. HRTF 3D Extension Positional (C-Media 3DX)

3D illusion exists because traditional 3D positional audio system assumes the user's position as the sweet spot to design crosstalk-cancellation circuit; therefore, if the user wants to have 3D positional audio effects, he can't move his head or position out of sweet spot. Another 3D illusion fails because half the population are compulsive "head-turners" who will never get 3D audio from two speakers . To remedy this, C-Media utilizes HRTF 3D extension technology (C3DX) to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four-speaker one. Therefore, at least one or two speakers should be placed behind the listener's head to complement the rear-side effect, thus creating compelling realistic sound. This technology greatly improves HRTF 3D positional audio quality, and successfully eliminates the sweet spot limitation. Users can enjoy the real 3D audio gaming effects, and don't have to worry about the environmental confinement any more.



C3D HRTF Positional Audio Technology

C3D technology uses an audio filter called Head Related Transfer Functions (HRTFs), which is licensed from CRL®(Central Research Lab). The basic concept of C3D is: since we can hear sound three dimensionally in the real world using our two ears, it must be possible to regenerate the same sound effect from two loud speakers.

What is HRTF ?

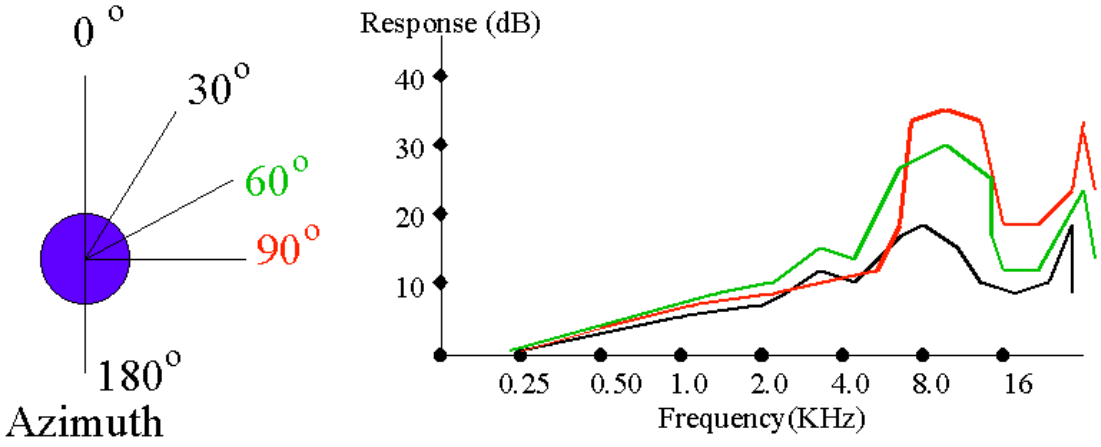
HRTF (Head Related Transfer Functions) is a set of audio filters which can vary locations of sound effects (spatial hearing cues) in three-dimension measured from the listener's eardrum.
People can use this technology and special digital signal processing to re-create spatial hearing cues, so as to makes the ears hear a realistic and three-dimensional sounds coming from a pairs of loud speakers or headphones.

There are several listening cues which allow people to hear sounds three-dimensionally :

(I). Spatial Hearing : Primary 3D-cues

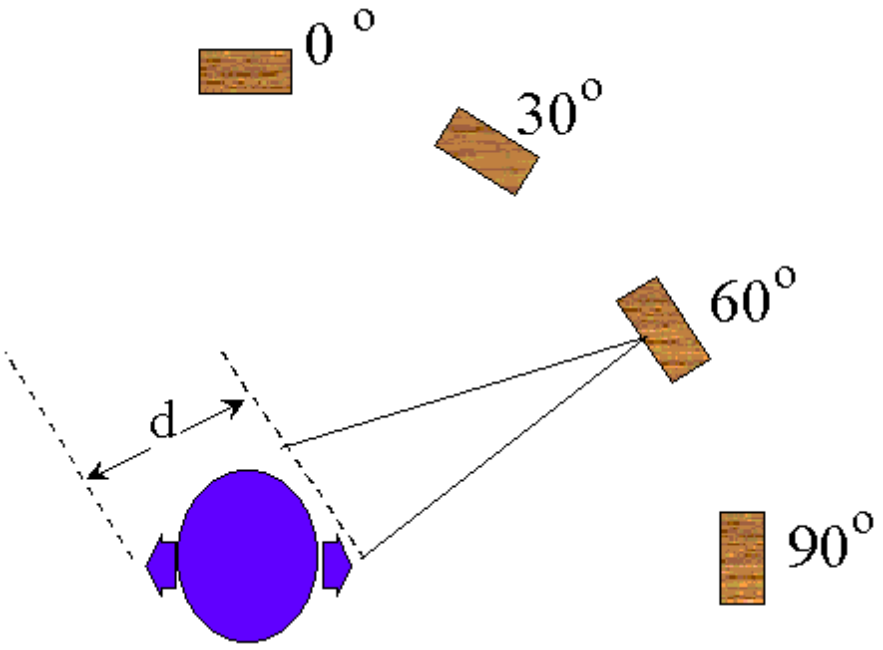
1. IAD

   The head shadowing effect creates differences in the amplitudes of the sound signals arriving at each ear from the source. The effects of diffraction are most noticeable in the range between about 700 Hz to 8 KHz, where the A and S functions periodically converge and diverge gently. This Inter-aural Amplitude difference (IAD) is one of the primary 3D sound cues.



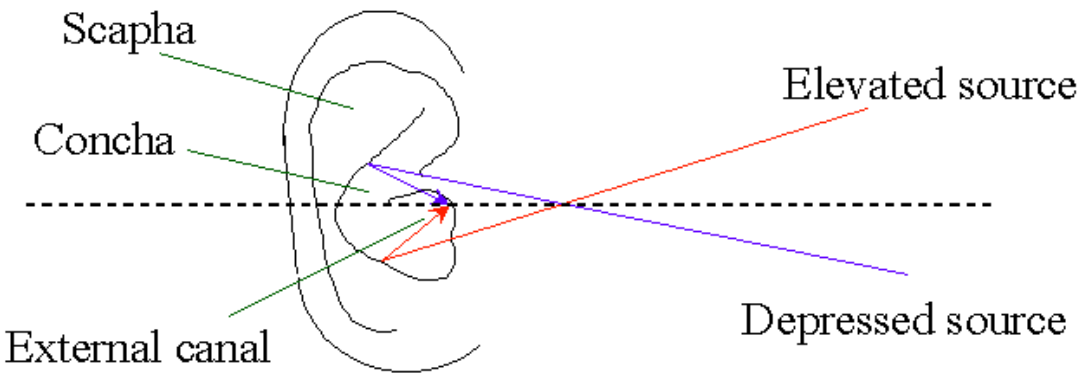
2. ITD

In addition to IAD, there is also a time-of-arrival difference between the left and right ears(unless the sound source is in one of the pole positions, such as directly in front, behind, above and below): this is known as the Inter-aural Time Delay (ITD).



3. Pinna Effects

It has been presumed by several researchers that the convolutions of the pinna create the spectral features which constitute the 'height' cues. In practical experiments by Gardner, in which different parts of the pinna were occluded, and then the ability of a number of subjects to identify sound source positions at different heights was tested, it was shown that the different features all contributed by different amounts. For example, if the fossa is excluded, then height localization capability is impaired, but not totally extinguished. It would be reasonable to conclude that it is the combined effect of the pinna convolutions which create the various localization cues, and it is not valid - or logical - to attempt to assign particular spatial capabilities with individual physical features.



(II). Spatial Hearing : Secondary 3D-cues (shoulder & local reflections)

In addition to the 'primary' 3D sound cues (IAD, ITD and pinna effects), there are several additional cues which do contribute to the localization capability; these will be referred to here as 'secondary' cues, and include shoulder/torso reflections, local room reflections, and psychological cues.

1. Shoulder / Torso reflections

The presence of a torso attached to an artificial head has the effect of increasing the pressure in the vicinity of the ear up to frequencies of around 2 kHz. The effect is greater for frontal sources than lateral ones. In experience, the presence of the torso does not appear to contribute much to spatial accuracy. However, shoulders are located very close to the ears, and their effect is greater, this time, in respect of

lateral sounds. If one listens to an artificial head first without - and then with - shoulder fitments, then it is clear that the shoulders do contribute to spatial effects in certain positions. The shoulders provide a strong reflection from lateral sources, with a short path-length of around 10 cm between direct sound and reflection. The effects are most important for side-positioned sources, especially for "height" effects, where the shoulders tend to mask sources which move below about 30 degree depression.

2. Local, Room Reflections

In simulations, it is clear that the incorporation of first-order simulated room reflections can help in the creation of sound images which have a "solid" nature. However, the effects - if accurately simulated - are relatively slight. Experience has shown that it is primarily the quality of the HRTFs themselves which determine the quality and solidity of the sound image. The further addition of second-order reflections does not help significantly, because in reality, there is a great number of reflections in the average room. A method which does help to recreate the acoustic experience of a room, however, is to use approximate simulations of lateral reverb, using either 2 or 4 laterally placed "virtual" sources at, say, +-70 degrees and 80 degrees azimuth.

- The quality of the sound image relates to the HRTFs used.
- The quality of the room image relates to addition of reflections and reverb.

3. Psychological Cues

There are clearly psychological cues present in everyday life which work together with the audio cues to tell us about the world around us. For example, if you hear the sound of a helicopter flying, you expect it to be up in the air, and not downwards. If a dog is barking nearby, you would expect it to be downwards.

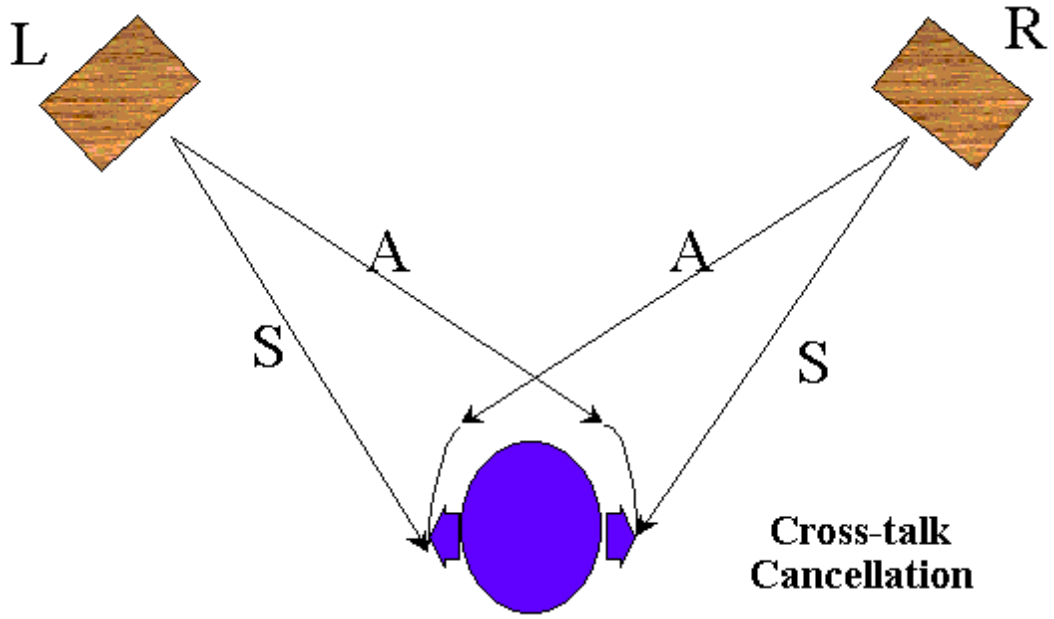
How to listen to C3D sound correctly and properly?

1. Use Headphones to Have Much Better Effect

When you use headphones in listening, there will be less interference such as outside voices or room reflections comparing to using speakers.

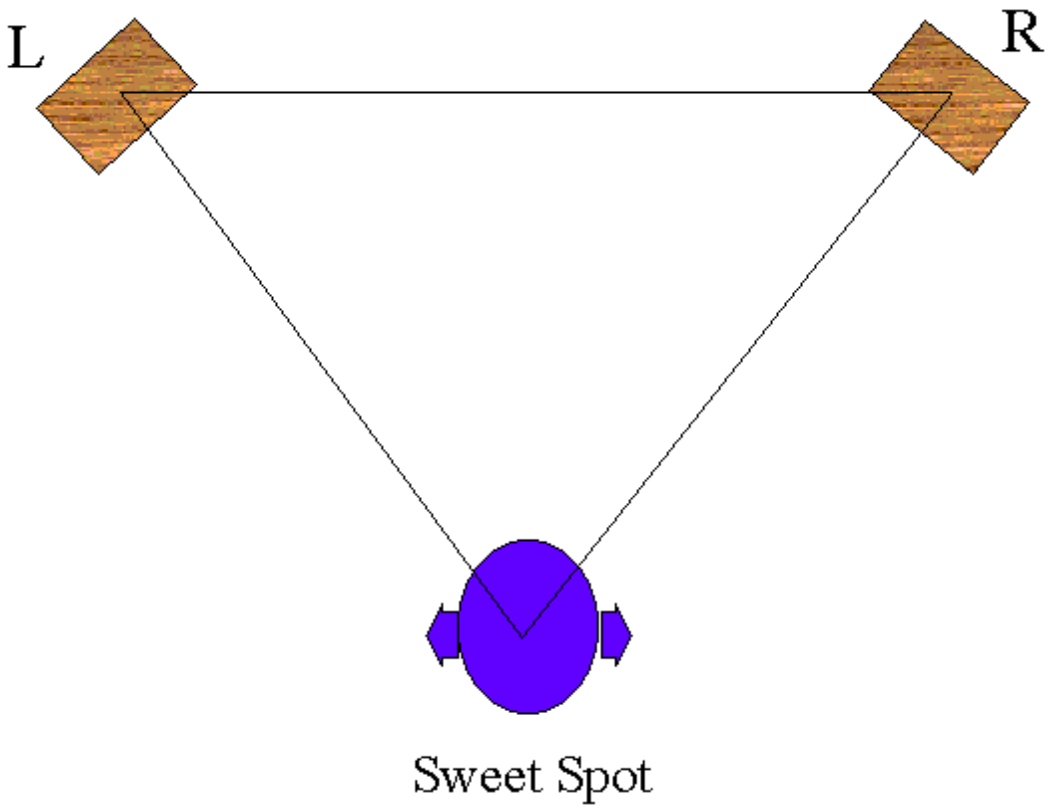
2. Choose Correct Output Devices

Choose the correct output devices in the options of demo program in accordance with what listening devices you want to listen to. Listening through speakers must be proceeded by crosstalk-cancellation, so if you choose the wrong output devices, there won't be any 3D positional audio effect.



3. Position of Speakers

If you listen from speakers, please do not reverse the left and right speakers, which should be put in equal distance from the listener. That is, the listener, the left, and the right speaker must be in the topmost of a right triangle. The position of the listener is called the “sweet spot”. In addition, the height of the listener’s ears must be equal to that of the speakers.

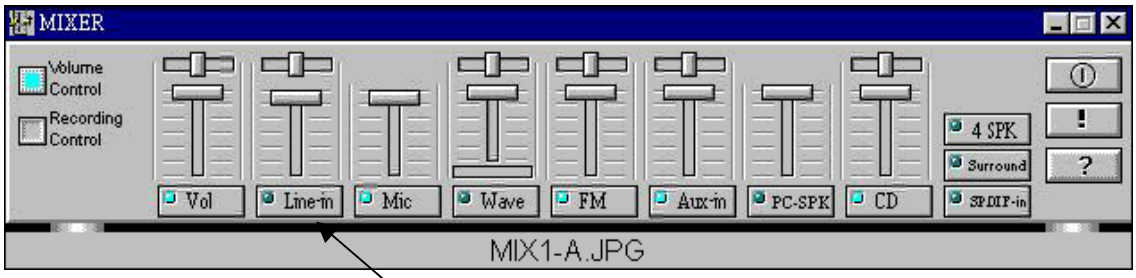


4. Turn Surround Sound Functions off

When the surround sound effect is enabled, it will cause confusion with C3D sound, and make positional sound effect invalid.

Audio Rack Panel

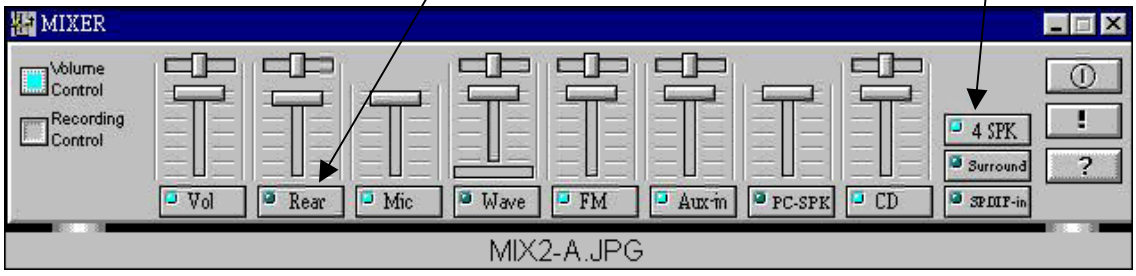
Two Speakers System :



Line-In becomes
Rear Speakers Output

4 Speakers
system Enable

Four Speakers System :



CMI8738 PCI Audio Adapter Layout Notes

1. The wires of analog circuits(chip pin64-80) must be wider than 12mil.
2. Placing digital signals such as SPDIF IN/OUT(pin86, 98) and TXD/RXD(pin88,89) near the analog signals should be avoided. However, if these signals have to be adjacent, please place ground between these digital and analog signal wires to isolate noises.
3. The whole PCB grounding should be well-organized(The ground must be placed as much as possible. Also, the ground of both the component and the solder sides should be drilled as much as possible.).
4. The grounding under CMI8738 should be well-organized as mentioned above.
5. The regulator(78L05) must be placed near the chip as much as possible.
6. The chip and the circuits need independent power supply regulators to prevent insufficient currents.

Revision release note:

V1.1 12/17/2001

1. Add register listing.

V1.2 01/17/2003

2. Add Pin62 XINTREF description.